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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/615,845	07/10/2003	Sterling Smith	MSS0003-US	9986

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Michael D. Bednarek
Shaw Pittman LLP
1650 Tysons Boulevard
McLean, VA 22102

EXAMINER	
VLAHOS, SOPHIA	
ART UNIT	**PAPER NUMBER**
2611	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/21/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/615,845	SMITH, STERLING	
	Examiner	Art Unit	
	SOPHIA VLAHOS	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 7-14* is/are rejected.

7)☒ Claim(s) *6, 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *7/10/2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The amendment to the specification (received on 12/04/2006) is acceptable.

Allowable Subject Matter

2. The indicated allowability of claims 1-15 is withdrawn in view of the newly discovered reference(s) to Mathe et. al. (U.S. 5,825,253) and Riley (U.S. 4,967,531). Rejections based on the newly cited reference(s) follow.

Claim Objections

3. Claims 5 and 14 are objected to because of the following informalities: Claims 5 and 14 (last limitation) recite: "... to said a period nominal." Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-4, 7-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Mathe et. al. (U.S.5, 825,253).

With respect to claim 1, Mathe et. al., disclose: a divider for receiving a reference clock with a substantially fixed period (see Fig. 2, variable divider block 104, receiving

clock from clock source 102 that has a substantially fixed period since it is the reference frequency (clock) source, column 5, lines 9-10) and generating an output clock with a time-varying period (see column 3, lines 31-33 (where the average frequency (period) is at the desired frequency (period)), and column 5, line 67 through column 6, lines 1-5, (where controlling the clock cycle of the event clock in non-periodic manner corresponds to the claimed output clock with a time-varying period (cycle)) where the divided reference clock (i.e. the "event clock" as shown in Fig. 2 corresponds to the generated output clock); a noise-shaped quantizer for quantizing a period control word to a time-varying value in response to said output clock fed from said divider (see Fig. 2, event clock is fed-back to block 120 "divider Controller" details of which are shown in Fig. 3 and Fig. 4, see Fig. 4, block 218 quantizer inside the sigma delta modulator where the period control word corresponds to the signal at the noise shaper input and the output is supplied to adder 160 (added with a coarse control) and the addition result is supplied as the control signal to the variable divider) so that said divider generates said output clock by means of dividing said reference clock by said time-varying value (see column 3, lines 30-34); means for adjusting said period control word by a period offset in response to said output clock (Fig. 4, subtractors 208a and 208b subtracting the delayed noise shaper output column 7, lines 35-40, 44-46); and a filter for substantially filtering out jitter from said output clock (Fig. 2, see event clock is supplied to PLL (blocks 106, 108.110. 112) see column 4, lines 39 see that the clock signal (output of PLL) has "good phase noise characteristics" i.e. the PLL "filters" out jitter of

the event clock (the claimed output clock) and supplies a clock signal with the "good phase noise characteristics").

With respect to claim 2, all of the limitations of claim 2 are analyzed above in claim 1, and Mathe et. al disclose: wherein said period control word has a bit resolution greater than that of said time-varying value (see column 11, lines 23-36 equation for p>=log2(M-1), where M is the division ratio , for example k=20, and see Fig. 2 where block 120 has k-bit input and p-bit output).

With respect to claim 3, all of the limitations of claim 3 are analyzed above in claim 1, and Mathe et. al., disclose: wherein said noise-shaped quantizer is a delta-sigma quantizer (see column 7, lines 28-30, where the shaper is a delta sigma shaper i.e. the quantizer is a delta-sigma quantizer).

With respect to claim 4, all of the limitations of claim 4, all of the limitations of claim 4 are analyzed above in claim 4, and Mathe et. al., disclose: wherein said filter is an analog phase locked loop (PLL) device as a low pass filter for removing high frequency jitter from said output clock (see column 4, lines 39-41, 49-56, and line 67 throught column 5, lines 1 (where the loop filter has a lowpass nature) and the PLL "filters" the input signal using the narrow loop bandwidth of the loop filter (LPF nature) and the VCXO, and see column 5, lines 24-26 for the analog PLL device).

Claims 7-13 are rejected under a similar rationale used to reject claims 1-4 above. Specifically claims 7-8 and 10-11 are rejected similarly to claim 1 above. Claims 9, 12, 13 are rejected similarly to claims 4, 2, 3 respectively.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-5, 7-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Riley (U.S. 4,965,531) in view Mathe et. al. (U.S. 5,825,253).

With respect to claim 1, Riley discloses: a divider for receiving a reference clock with a substantially fixed period and generating an output clock with a time-varying period (see Fig. 4, where the reference frequency fr corresponds to the reference clock with substantially fixed period and fod corresponds to the clock with a time-varying period since the divider 106 is controlled by signal the time varying signal b(t) out of the sigma-delta modulator 102, and the output clock has time varying frequency (period) since fr is divided by n , n+1 (see column 4,lines 66-67,column 5, lines 1-2 describing similar functions of the system shown in Fig. 2); a noise-shaped quantizer for quantizing a period control word to a time-varying value in response to said output clock fed from said divider so that said divider generates said output clock by means of dividing said reference clock by said time-varying value (see sigma-delta modulator 102 which is a

noise-shaped quantizer since b(t) that includes quantization noise is fed-back to control mux 206 (where quantization noise is inherent in b(t) see column 5, lines 38-40), the period control words is signal δΦ (see Fig. 4)(see column 3, lines 22 where δΦ is the frequency (period) control signal) time varying signal b(t) shown in Fig, 4 (and the corresponding parts of Fig. 2) and see column 5, lines 38-40, where b(t) is a quantized 1-bit signal); means for adjusting said period control word by a period offset in response to said output clock (the claimed means corresponds to mux 204 and blocks 208, 210 that are part of the sigma-delta modulator, see Fig. 2 where b(t) s fed-back to mux 206 and selects "+Ref" or "–Ref" (the frequency (period) offset) supplied to adder 202, and the period offset is generated in response to fd (fod output clock for Fig. 4) since b(t) is generated in response to fd (since elements 214, 215, 218 that generate b(t) are clocked (function in response to fd) with fd);

Riley does not expressly teach: a filter for substantially filtering out jitter from said output clock.

In the same field of endeavor Mathe et. al., disclose: a filter for substantially filtering out jitter from output clock (see Fig. 2, PLL comprising elements 106, 108, 110, 112 filtering the "event clock", see column 4, lines 35-67, column 5, line 1).

At the time of the invention, it would have been obvious to a person skilled in the art to modify the system of Riley so that it includes a filter for substantially filtering out jitter from output clock (as taught by Mathe et. al.,) and the motivation for incorporating the filter of Riley in the system of Riely would be to obtain good phase noise characteristics in the clock signal (see column 4, lines 51-52 of Mathe et. al.,).

With respect to claim 2, all of the limitations of claim 2, are analyzed above in claim 1, and Riley discloses: wherein said period control word has a bit resolution greater than that of said time-varying value (column 5, lines 38-40, where the output of the sigma-delta modulator, ie. b(t) has 1-bit resolution, whereas signal $\delta\Phi$ has more bits, ie. is a high resolution input).

With respect to claim 3, all of the limitations of claim 3, are analyzed above in claim 1, and Riley discloses: wherein said noise-shaped quantizer is a delta-sigma quantizer (Fig. 4, block 102, delta-sigma modulator that performs quantization).

With respect to claim 4, all of the limitations of claim 4 are analyzed above in claim 1.

With respect to claim 5, all of the limitations of claim 5 are analyzed above in claim 1, and Riley discloses: wherein said means for adjusting said period control word comprises: an offset generator for generating said period offset in response to said output clock (see mux 204 that "generates" the offset when it selects the :+Ref" or "-Ref", and blocks 208, 210 that are part of the sigma-delta modulator, see Fig. 2 and b(t) controls the mux therefore the period offset is generated in response to fd (fod output clock for Fig. 4) since b(t) is generated in response to fd (see elements 214, 215, 218 that generate b(t) are clocked (function in response to fd) with fd) ; and an adder for

generating said adjusted period control word by means of adding said period offset to said a period nominal (see Fig. 2, adder 202).

Claims 7-14 are rejected under a similar rationale used to reject claims 1-5 above. Specifically claims 7-8 and 10-11 are rejected similarly to claim 1 above. Claims 9, 12, 13, 14 are rejected similarly to claims 4, 2, 3, 5 respectively.

Allowable Subject Matter

8. Claims 6, 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SOPHIA VLAHOS whose telephone number is 571 272 5507. The examiner can normally be reached on MTWRF 8:30-17:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammed Ghayour can be reached on 571 272 3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SV
2/7/2007

MOHAMMED GHAYOUR
SUPERVISORY PATENT EXAMINER